AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A memory module including a non-volatile memory, a dynamic random access memory, a static random access memory, and a control circuit that accesses the non-volatile memory, the dynamic random access memory, and the static random access memory, the memory module comprising:

a dynamic random access memory interface to outside the memory module for accessing the dynamic random access memory from ~~a device~~ outside the memory module; and

a static random access memory interface to outside the memory module for accessing the static random access memory from outside the memory module.

2. (original) A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the static random access memory.

3. (original) A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the dynamic random access memory.

4. (currently amended) A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the dynamic random access memory is performed according to an instruction sent via the dynamic random access memory interface.

5. (currently amended) A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the static random access memory is performed according to an instruction sent via the static random access memory interface.

6. (currently amended) A memory module according to Claim 1, wherein:

in transferring data ~~transfer~~ from the non-volatile memory to the static random access memory or the dynamic random access memory, data ~~acquired by correcting~~ having an error is corrected before being transferred.

7. (currently amended) A memory module according to Claim 1, wherein:

in transferring data ~~transfer~~ from the static random access memory or the dynamic random access memory to the non-volatile memory, an address replacement process is executed.

8. (original) A memory module according to Claim 1, wherein:

a boot program is held in the non-volatile memory.

9. (currently amended) A memory module according to Claim 1, wherein:

data transfer range data, which includes ~~showing~~ a range of data transferred from the non-volatile memory to the dynamic random access memory at initial time when operating power is turned on, is held in the non-volatile memory.

10. (currently amended) A memory module according to Claim 1, wherein:

~~the non-volatile memory and the dynamic random access memory have the similar memory size; and~~

the static random access memory has a memory size equal ~~to/smaller~~ to or smaller than 1/1000 of ~~that~~ the memory size of the non-volatile memory.

Claim 11. (cancelled)

12. (currently amended) A memory module according to Claim 1, wherein:

~~the~~ a data-hold operation of the dynamic random access memory is executed inside the memory module.

Claim 13. (cancelled)

14. (currently amended) A memory module according to Claim 12[[1]], wherein:

~~access from the device outside~~ the memory module is accessed first;~~is first preceded;~~

the dynamic random access memory performs a data-hold operation second; and ~~of the dynamic random access memory inside the memory module is second preceded; and~~

the memory module performs data transfer between the non-volatile memory and the static random access memory or the dynamic random access memory [[is]] third ~~preceded~~.

15. (currently amended) A memory module according to Claim 1, wherein:

the dynamic random access memory is synchronous DRAM; and

access to the non-volatile memory and the dynamic random access memory from ~~the device~~ outside the memory module is made via ~~an interface of the synchronous DRAM~~ the dynamic random memory access interface.

16. (original) A memory module according to Claim 1, wherein:

the non-volatile memory is a NAND flash memory; and

the dynamic random access memory is synchronous DRAM.

17. (original) A memory module according to Claim 1, wherein:

the non-volatile memory is an AND flash memory; and

the dynamic random access memory is synchronous DRAM.

Claim 18-20. (cancelled)

21. (currently amended) A memory module according to Claim 1, wherein:

the dynamic random access memory ~~is equipped with~~ includes plural interfaces.

Claims 22-23 (cancelled)

24. (currently amended) A memory module according to Claim 1, wherein:

the dynamic random access memory ~~is equipped with~~ includes a control circuit ~~for processing~~ which processes access from the ~~device~~ outside of the memory module and a control circuit ~~for~~ that independently ~~accessing~~ accesses the non-volatile memory.

25. (currently amended) A memory module according to Claim 1, wherein:

the dynamic random access memory ~~is equipped with~~ includes a control circuit ~~for independently accessing~~ to independently access the non-volatile memory and a circuit ~~for subordinately processing~~ to subordinately process the access.

Claim 26. (cancelled)

27. (currently amended) A memory module according to Claim 1, wherein:

the non-volatile memory ~~is equipped with~~ includes a static random access memory, an error detecting and correcting circuit, and an address replacement circuit.

28. (currently amended) A memory module according to Claim 1, wherein:

the non-volatile memory ~~is equipped with~~ includes plural interfaces.

Claims 29-78. (cancelled)

79. (new) A memory module according to Claim 1, wherein:

said accessing the dynamic random access memory is from a device outside the memory module.